AND8281/D

Implementing the NCP1605 to Drive the PFC Stage of a 19 V / 8 A Power Supply

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APPLICATION NOTE

Forward or half−bridge converters take a significant advantage of a narrow input voltage range. In such applications, the PFC stage is wished to start first and to keep on as long as the power supply is plugged in. Optimally, the downstream converter should turn on when the output of the PFC stage is nominal. ***In other words, the PFC must be the master***…

The NCP1605 is specially designed for these applications. It features a "pfcOK" pin to enable the downstream converter when the PFC stage is ready for operation. Practically, it is in high state when the PFC stage is in steady state and low otherwise (fault or start−up condition). In addition, the PFC stage having to still remain active in light load conditions, the NCP1605 integrates the skip cycle capability to lower the stand−by losses to a minimum.

This application note shows how to design a NCP1605 PFC driven. The dimensioning criteria / equations are presented in a general manner but for the sake of clarity, this process is illustrated in the following practical application:

- Ac line range: 90 V up to 265 V
- Output Voltage: 19 V / 8 A
- IEC61000−3−2 Class D compliant

The power supply consists of two stages:

- A PFC pre−converter driven by the NCP1605
- The main power supply: 2 switches forward driven by the NCP1217A, 133 kHz

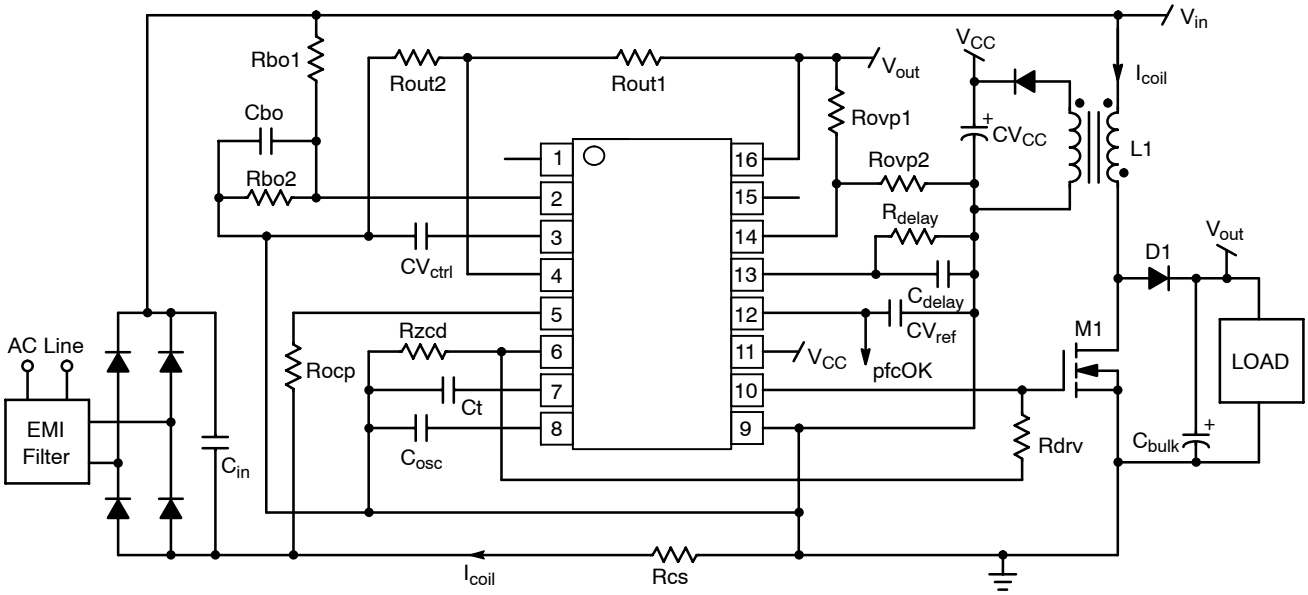

Figure 1. Generic Application Schematic

The "pfcOK" signal enables the downstream converter when the PFC is ready

Introduction

The NCP1605 is a PFC driver designed to operate in fixed frequency, Discontinuous Conduction Mode (DCM). In the most stressful conditions, Critical Conduction Mode (CRM) can be achieved without power factor degradation and the circuit could be viewed as a CRM controller with a frequency clamp (given by the oscillator). Finally, the NCP1605 tends to give the best of both modes without their respective drawbacks. Furthermore, the circuit incorporates protection features for a rugged operation together with some special circuitry to lower the power consumed by the PFC stage in no load conditions. More generally, the NCP1605 functions make it the ideal candidate in systems where cost−effectiveness, reliability, low stand−by power and high power factor are the key parameters:

- **Compactness and Flexibility:** the controller requires few external components while offering a large variety of functions. Depending on the selected coil and oscillator frequency you select, the circuit can:
  1. Mostly operate in Critical Conduction Mode and use the oscillator as a frequency clamp.
  2. Mostly operate in fixed frequency mode and only run in CRM at high load and low line.
  3. Permanently operate in fixed frequency mode (DCM).

In all cases, the circuit provides near−unity power factor.

- **Skip−cycle Capability for Low Power Stand−by:** among other applications, the circuit targets power supply where the PFC stage must keep alive even in stand−by. A continuous flow of pulses is not compatible with no−load standby power requirements. Instead, the controller slices the switching pattern in bunch of pulses to drastically reduce the overall losses. The skip cycle operation is initiated by applying to pin 1, a signal that goes below 300 mV in stand−by. Typically, this signal is drawn from the feed−back of the downstream converter.
- **Start−up Current Source and Large V_{CC} Range:** meeting low stand−by power specifications represents a difficult exercise when the controller requires an external, lossy resistor connected to the bulk capacitor. The controller disables the high−voltage current source after start−up which no longer hampers the consumption in no−load situations. In addition, the large V_{CC} range (10 V to 20 V after start−up), highly eases the circuit biasing.
- **Fast Line / Load Transient Compensation:** given the low bandwidth of the regulation block, the output voltage of PFC stages may exhibit excessive over and under−shoots because of abrupt load or input voltage variations (e.g. at start−up). If the output voltage is too far from the regulation level:
  - The NCP1605 disables the drive to stop delivering power as long as the output voltage exceeds the over voltage protection (OVP) level.
  - The NCP1605 drastically speeds up the regulation loop when the output voltage is below 95.5% of its regulation level. This function is allowed only after the PFC stage has started up not to eliminate the soft−start effect.
- **PFC OK:** the circuit detects when the circuit is in normal situation or if on the contrary, it is in a start−up or fault condition. In the first case, pin12 is in high state and low otherwise. Pin12 serves to control the down−stream converter operation in response to the PFC state.
- **Safety Protections:** the NCP1605 permanently monitors the input and output voltages, the coil current and the die temperature to protect the system from possible over−stresses and make the PFC stage extremely robust and reliable. In addition to the aforementioned OVP protection, one can list:
  - **Maximum Current Limit and Zero Current Detection:** the circuit permanently senses the coil current and immediately turns off the power switch if it is higher than the set current limit. It also prevents any turn on of the power switch as long as some current flows through the coil, to ensure operation in discontinuous conduction mode. This feature also protects the MOSFET from the excessive stress that could result from the large in−rush currents that occurs during the start−up phases.
  - **Under−Voltage Protection:** the circuit turns off when it detects that the output voltage goes below 12% of the OVP level (typically). This feature protects the PFC stage from starting operation in case of too low ac line conditions or in case of a failure in the OVP monitoring network (e.g., bad connection).
  - **Brown−Out Detection:** the circuit detects too low ac line conditions and stop operating in this case. This protection protects the PFC stage from the excessive stress that could damage it in such conditions.
  - **Thermal Shutdown:** an internal thermal circuitry disables the circuit gate drive and then keeps the power switch off when the junction temperature exceeds 150°C typically. The circuit resumes operation once the temperature drops below about 100°C (50°C hysteresis).
- **Output Stage Totem Pole:** the NCP1605 incorporates a −0.5 A / +0.8 A gate driver to efficiently drive most TO220 or TO247 power MOSFETs.

Design of the PFC Stage

Power Components

The selection of the oscillator frequency is a prerequisite step before dimensioning the PFC stage. For this application, we choose to clamp the switching frequency at around 130 kHz because this frequency is generally a good trade−off when considering the following aspects:

- A high switching frequency reduces the size of the storage elements. In particular, it is well known that the higher the switching frequency, the lower the transformer core. That is why, one should set the switching frequency as high as possible,
- On the other hand, increasing the switching frequency has two major drawbacks:
  - The switching rate increasing, the associated losses grow up. In addition, all parasitic capacitors charge at a higher frequency and generate more heat…
  - EMI filtering is tougher: the switching generates high EMI rays at the switching frequency and close harmonic levels. Most power supplies have to meet the CISPR22 standard that applies to frequencies above 150 kHz. That is why SMPS designers often select F_{SW} = 130 kHz so that the fundamental keeps below 150 kHz and then out of the regulation scope. Often, 65 kHz is also chosen to not to have to damp harmonic 2 too.

The oscillator frequency will then be set to approximately 130 kHz.

Coil Selection

The coil is selected so that CRM operation is achieved in the most stressful conditions (full power, low line). In other words, its inductance must be large enough not to have dead−times at least at the top of the sine−wave.

In CRM, the coil peak current is:

$$I_{coil,max} = 2 \cdot \sqrt{2} \cdot \frac{P_{in,av}}{V_{in,rms}} \qquad \text{(eq. 1)}$$

The coil current ramps up to its peak value during the MOSFET on−time and then ramps down to zero during the diode conduction period (coil demagnetization time). In CRM, this cycle time must be longer than the oscillator period.

The on−time duration is:

$$T_{on} = \frac{L \cdot I_{coil,pk}}{V_{in}} \qquad \text{(eq. 2)}$$

The demagnetization time is:

$$T_{demag} = \frac{L \cdot I_{coil,pk}}{V_{out} - V_{in}}$$

Hence the total current cycle time is:

$$T_{cycle} = T_{on} + T_{demag} = \frac{L \cdot I_{coil,pk} \cdot V_{out}}{V_{in} \cdot (V_{out} - V_{in})} \qquad \text{(eq. 3)}$$

The necessity of having a cycle time longer than the oscillator period when at low line, the coil current is maximal, leads to:

$$\frac{L \cdot I_{coil,max} \cdot V_{out}}{V_{in,pk} \cdot (V_{out} - V_{in,pk})} > T_{osc} \qquad \text{(eq. 4)}$$

Substitution of equation (1) into inequation (4) leads to:

$$L > T_{osc} \cdot \frac{V_{in,pk}^{\,2} \cdot (V_{out} - V_{in,pk})}{4 \cdot P_{IN,AVG} \cdot V_{out}} \qquad \text{(eq. 5)}$$

In our application,

- T_{osc} = 7.5 μs (133 kHz)
- $V_{in,pk}$ = 127 V ($\sqrt{2} \cdot 90$ V)
- V_{out} = 390 V
- $P_{IN,AVG}$ = 190 W (80% global efficiency)

Hence,

$$L > 7.5 \cdot \frac{127^2 \cdot (390 - 127)}{4 \cdot 190 \cdot 390}\ \mu H = 107\ \mu H$$

In order to have a significant margin, a 150 μH coil is selected.

As in the most stressful conditions, the PFC stage operates in CRM, the rms and peak coil currents are calculated as they would be computed with a full CRM circuit.

- Maximum Peak Current:

$$I_{coil,max} = 2 \cdot \sqrt{2} \cdot \frac{(P_{IN,AVG})max}{V_{IN,rms,LL}} \qquad \text{(eq. 6)}$$

- RMS Coil Current:

$$I_{coil,rms} = \frac{2}{\sqrt{3}} \cdot \frac{(P_{IN,AVG})max}{V_{IN,rms,LL}} \qquad \text{(eq. 7)}$$

Finally, the coil specification is:

- L = 150 μH
- $I_{coil,max}$ = 6.0 A
- $I_{coil,rms}$ = 2.5 A

MOSFET and Diode Selection

The following equation gives the MOSFET conduction losses (refer to the AND8123 application note available at http://www.onsemi.com/pub/Collateral/AND8123−D.PDF for further information):

$$p_{on} = \frac{4}{3} \cdot R_{dsON} \cdot \left(\frac{P_{in,av}}{V_{in,rms}}\right)^2 \cdot \left[1 - \frac{8 \cdot \sqrt{2} \cdot V_{in,rms}}{3\pi \cdot V_{out}}\right] \qquad \text{(eq. 8)}$$

Hence, the losses are maximal at low line and full load. In our application, we can evaluate them as follows:

$$(p_{on})max = \frac{4}{3} \cdot R_{dsON} \cdot \left(\frac{190}{90}\right)^2 \cdot \left[1 - \frac{8 \cdot \sqrt{2} \cdot 90}{3\pi \cdot 390}\right] \cong 4.3 \cdot R_{dsON} \qquad \text{(eq. 9)}$$

In our application, we use a MOSFET that according to the data sheet, exhibits a 0.4 Ω on−time resistance at 150°C. Hence:

$$(P_{on})max \cong 1.7\ W \qquad \text{(eq. 10)}$$

The switching losses are more difficult to compute. As a rule of the thumb, we generally reserve a loss budget equal to that of the conduction ones. One can anyway note that the NCP1605 limits this source of dissipation by clamping the switching frequency (that can never exceed the oscillator one − 133 kHz in our case). To further improve the efficiency, the MOSFET opening can be accelerated using the schematic of Figure 2, where the Q2 npn transistor (TO92) amplifies the MOSFET turn off gate current.

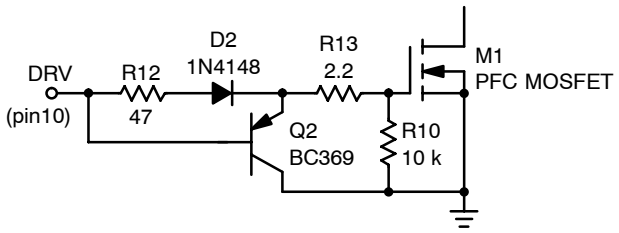

Figure 2. Q2 Makes Steeper the Turn Off

Bulk Capacitor

The main criteria / constraints in the bulk capacitor choice are generally:

1. Peak to peak Low Frequency Ripple:

$$(\delta V_{OUT})_{pk-pk} = \frac{\eta \cdot (P_{IN,AVG})_{max}}{C_{BULK} \cdot \omega \cdot V_{OUT,nom}} \qquad \text{(eq. 11)}$$

where ω is the ac line angular frequency. This ripple must typically keep lower than 5% of the output voltage. This leads to:

$$C_{BULK} \geq \frac{94\% \cdot 190}{5\% \cdot 2\pi \cdot 100 \cdot 390^2} = 37\ \mu F \qquad \text{(eq. 12)}$$

2. Hold−up time specification:

$$C_{BULK} \geq \frac{\eta \cdot (P_{IN,AVG})_{max} \cdot t_{HOLD-UP}}{V_{OUT,nom}{}^2 - V_{OUT,min}{}^2}. \qquad \text{(eq. 13)}$$

Hence, a 10 ms hold−up time imposes:

$$C_{BULK} \geq \frac{94\% \cdot 190 \cdot 10\ m}{390^2 - 350^2} \cong 65\ \mu F \qquad \text{(eq. 14)}$$

3. RMS capacitor Current:

$$I_{C,rms} = \sqrt{\left[\frac{32 \cdot \sqrt{2}}{9\pi} \cdot \frac{P_{IN,AVG}{}^2}{V_{IN,rms} \cdot V_{OUT,nom}}\right] - \left(\frac{\eta_{PFC} \cdot P_{IN,AVG}}{V_{OUT,nom}}\right)^2} \qquad \text{(eq. 15)}$$

We will consider that η_{PFC} (η_{PFC} is the PFC efficiency) is 94% in the most severe conditions where this rms current is maximal (low line, full load). Finally:

$$I_{C,rms} = \sqrt{\left[\frac{32 \cdot \sqrt{2}}{9\pi} \cdot \frac{190^2}{90 \cdot 390}\right] - \left(\frac{94\% \cdot 190}{390}\right)^2} \cong \sqrt{1.646 - 0.210} \cong 1.2\ A \qquad \text{(eq. 16)}$$

Oscillator Frequency Setting

The oscillator frequency is given by the following formula:

$$f_{OSC} = \frac{840\ pF}{C_{pin8} + 20\ pF} \cdot 60\ kHz \qquad \text{(eq. 17)}$$

Hence, the pin8 capacitor must be selected in accordance to the following expression:

$$C_{pin8} = \frac{840\ pF \cdot 60\ kHz}{f_{OSC}} - 20\ pF \qquad \text{(eq. 18)}$$

In our application, we target 130 kHz, then:

$$C_{pin8} = 359\ pF \qquad \text{(eq. 19)}$$

Instead, a normalized 330 pF capacitor is chosen that leads to a 140 kHz frequency.

Brown−out Circuitry

The brown−out terminal (pin2) receives a portion of the PFC input voltage (V_{IN}). As during the PFC operation, V_{IN} is a rectified sinusoid, a capacitor must integrate the ac line ripple so that a portion of the (V_{IN}) average value is applied to the brown−out pin.

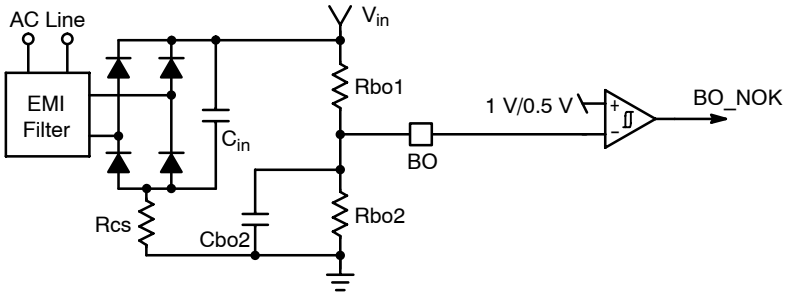

Figure 3. Brown−out Block

"BO_NOK" disables the NCP1605 drive when high.

As sketched by Figure 3, a portion of the average input voltage should be applied to pin2. The NCP1605 incorporates a comparator to monitor V_{pin2} and inhibits the circuit when this voltage is lower than the internal brown−out threshold. More specifically, the internal comparator features a 50% hysteresis ($V_{BO}L$ = 50% $V_{BO}H$) to take into account the change in the input voltage average level:

1. Before operation, the PFC stage is off and the input bridge acts as a peak detector (refer to Figure 4). As a consequence, the input voltage is approximately flat and nearly equates the ac line amplitude. Hence, the voltage applied to pin 2 is:

$$V_{pin2} = \sqrt{2} \cdot V_{in,rms} \cdot \frac{Rbo2}{Rbo1 + Rbo2}.$$

The PFC can start operation when Vpin2 exceeds "$V_{BO}H$" that is about 1 V.

2. After the PFC stage has started operation, the input voltage becomes a rectified sinusoid and the voltage applied to pin2 is:

$$V_{pin2} = \frac{2 \cdot \sqrt{2} \cdot V_{in,rms}}{\pi} \frac{Rbo2}{Rbo1 + Rbo2},$$

i.e., about 64% of the previous value. Therefore, the same line magnitude leads to a Vpin2 voltage that is 36% lower when the PFC is working than when it is off. The PFC stops operating if this Vpin2 level goes below "$V_{BO}L$" that is 0.5 V typically.

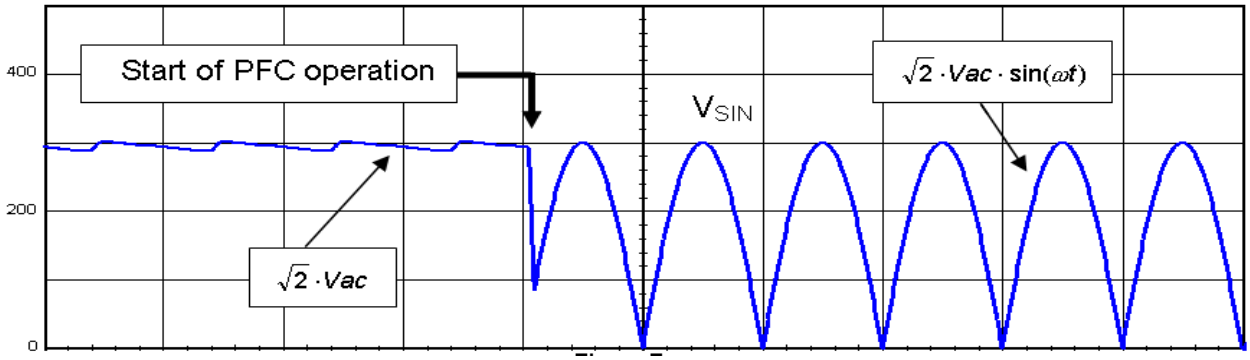

Figure 4. Typical Input Voltage of a PFC Stage

Computation of Rbo1, Rbo2, Cbo2:

Rbo1 and Rbo2 should be selected so that Vpin2 is 1 V at the lowest line voltage at which the PFC stage is allowed to start operation. Hence:

$$\frac{Rbo2}{Rbo1 + Rbo2} \cdot \sqrt{2} \cdot V_{in,rms,LL} = 1 \rightarrow \quad \text{(eq. 20)}$$

$$\frac{Rbo1}{Rbo2} = \sqrt{2} \cdot V_{in,rms,LL} - 1$$

Rbo2 is generally chosen in the range of 50 kΩ to minimize the leakage current to about 10 μA at low line.

The capacitor Cbo2 must be high enough to make V_{pin2} a dc voltage proportional to the line average value. Practically, select: [(Rbo1//Rbo2) · Cbo] in the range of half a line period.

In our case, 90 V_{rms} being the low level of our specification, let's take 85 V_{rms} to have some headroom.

Hence, following the aforementioned procedure:

$$Rbo2 = 56\ k\Omega$$
$$Rbo1 = 56\ k \cdot \sqrt{2} \cdot 85 \cong 6732\ k\Omega$$
$$Cbo = 220\ nF$$

Practically, four 1.8 MΩ are placed in series for Rbo1 (for safety reasons it is preferable to have several series resistors when applied to a high voltage rail), what leads to Rbo1 = 7200 kΩ instead of 6732 kΩ. Rbo2 is increased in the same ratio to 62 kΩ so that finally, the BO thresholds are:

$$(V_{in,rms})_{BO\_H} = \frac{Rbo1 + Rbo2}{Rbo2} \cdot \frac{1\ V}{\sqrt{2}} = 83\ V \quad \text{(eq. 21)}$$

$$(V_{in,rms})_{BO\_L} = \frac{Rbo1 + Rbo2}{Rbo2} \cdot \frac{\pi \cdot 0.5\ V}{2 \cdot \sqrt{2}} = 0.78 \cdot (V_{in,rms})_{BO\_H} = 65\ V \quad \text{(eq. 22)}$$

When a brown−out condition is detected, the signal "BO_NOK" turns off the circuit (refer to block diagram of the NCP1605 data sheet).

Remark: the calculated $(V_{IN,RMS})_{BO-L}$ is computed assuming that the voltage applied to the BO pin is a dc voltage devoid of ripple. In practice, the (Rbo1, Rbo2, Cbo2) network does not fully integrate the 100 or 120 Hz ripple of the rectified input rail so that the BO signal actually consists of some ac component that is superimposed to its dc voltage. These variations of the BO voltage make Vpin2 go to lower voltages at a given line amplitude and thus, make the BO comparator trigger at a higher line magnitude. The larger ripple, the higher $(V_{IN,RMS})_{BO-L}$. In other words, Cbo2 can be adjusted to set the wished $(V_{IN,RMS})_{BO-L}$.

Feed−back Network

The NCP1605 embeds a trans−conductance error amplifier that typically features a 200 μS trans−conductance gain and a ±20 μA maximum capability. The output voltage of the PFC stage is externally scaled down by a resistors divider and monitored by the feed−back input (pin4). The bias current is minimized (less than 500 nA) to allow the use of a high impedance feed−back network. The output of the error amplifier is pinned out for external loop compensation (pin 3).

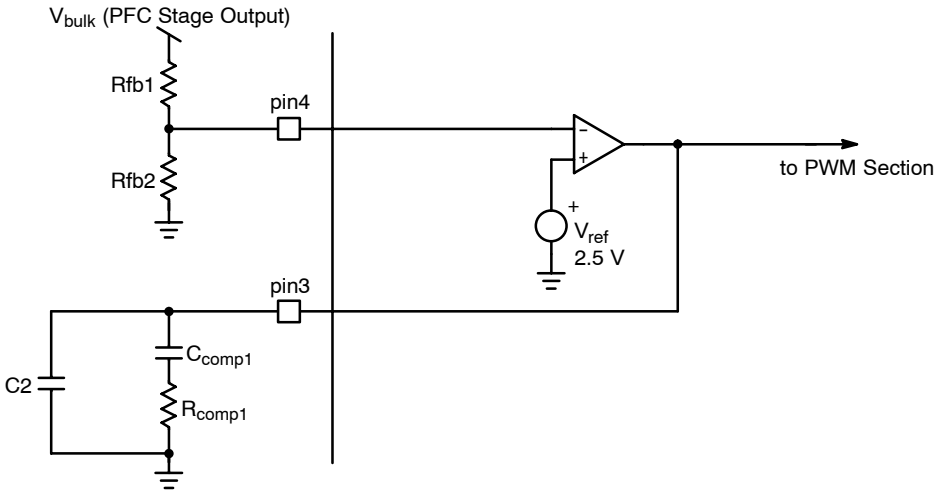

Figure 5. Regulation Trans−conductance Error Amplifier, Feed−back and Compensation Network

Computation of the Feed−back / Regulation External Components

A resistor divider consisting of Rfb1 and Rfb2 of Figure 5 must provide pin4 with a voltage proportional to the PFC output voltage so that Vpin3 equates the internal reference voltage (V_{REF} = 2.5 V) when the PFC output voltage is nominal. In other words:

$$\frac{Rfb2}{Rfb1 + Rfb2} \cdot V_{out,nom} = V_{REF} \rightarrow \frac{Rfb1}{Rfb2} = \frac{V_{out,nom}}{V_{REF}} - 1 \quad \text{(eq. 23)}$$

Another constraint on the feed−back resistors is the power it dissipates. Rfb1 and Rfb2 being biased by the PFC output high voltage (in the range of 400 V typically), they can easily consume several hundreds of mW if their resistance is low. Targeting a bias current in the range of 100 μA generally gives a good trade−off between wasted energy and noise immunity.

That means that:

$$Rfb2 = \frac{V_{REF}}{100\ \mu A} = 25\ k\Omega \quad \text{(eq. 24)}$$

In practice, we can choose:

$$Rfb2 = 27\ k\Omega \quad \text{(eq. 25)}$$

(instead of 25 kΩ, 27 kΩ being a normalized value)

Finally,

$$Rfb2 = 27\ k\Omega \quad \text{(eq. 26)}$$

$$Rfb1 = Rfb2 \cdot \left(\frac{V_{out,nom}}{V_{REF}} - 1\right) \quad \text{(eq. 27)}$$

In our application, we target a regulation level around 390 V.

Hence,

$$Rfb2 = 27\ k\Omega \quad \text{(eq. 28)}$$

$$Rfb1 = 27\ k\Omega \cdot \left(\frac{390}{2.5} - 1\right) = 4185\ k\Omega \quad \text{(eq. 29)}$$

Like for the input voltage sensing network, several resistors should be placed in series instead of a single Rfb1 resistor. In our application, we choose a **(1800 kΩ + 1800 kΩ + 560 kΩ = 4160 kΩ)** network. This selection together with **(Rfb2 = 27 kΩ)** leads to:

$$V_{out,nom} = \frac{Rfb1 + Rfb2}{Rfb2} \cdot V_{REF} = \frac{1800\ k + 1800\ k + 560\ k + 27\ k}{27\ k} \cdot 2.5\ V = 387.7\ V \quad \text{(eq. 30)}$$

Compensation:

The NCP1605 integrates the Follower Boost by making the charge current of the timing capacitor, a function of the squared output voltage. Based on the data−sheet equations and neglecting the zero resulting from the ESR of the bulk capacitor, a small signal analysis would lead to the following transfer function of the PFC stage:

$$\frac{V_{OUT}}{V_{REGUL}} = \left(\frac{Rfb1 + Rfb2}{Rfb2}\right)^2 \cdot \frac{C_{pin7} \cdot R_{LOAD} \cdot {V_{IN,RMS}}^2}{120\ \mu \cdot L \cdot {V_{OUT}}^2} \cdot \frac{1}{1 + \left[s \cdot \left(\frac{R_{OUT} \cdot C_{BULK}}{4}\right)\right]} \quad \text{(eq. 31)}$$

Where:

- C_{BULK} is the bulk capacitor
- R_{OUT} is the load equivalent resistance
- Cpin7 is the pin7 external capacitor
- L is the PFC coil inductance
- R_{fb1} and R_{fb2} are the feed−back resistors
- V_{REGUL} is the internal signal that generated by the regulation block modulates the MOSFET conduction time.
- R_{LOAD} is the equivalent load resistance.

However, PFC stages must exhibit a very low regulation bandwidth, in the range of 20 Hz to yield high power factor ratios. Hence, sharp variations of the load generally result in excessive over and under−shoots. The NCP1605 limits over−shoots by the Over−Voltage Protection (see OVP section). To contain under−shoots, an internal comparator monitors the feed−back (Vpin4) and when Vpin4 is lower than 95.5% of its nominal value, it connects a 220 μA current source to speed−up the charge of the compensation capacitor (Cpin3). Finally, it is like if the comparator multiplied the error amplifier gain by about 10 (Note 1).

The implementation of this ***dynamic response enhancer*** together with the accurate and programmable over−voltage protection, guarantees a reduced spread of the output voltage in all conditions included sharp line / load transients.

Hence, in most applications, it is sufficient to place a low frequency pole that drastically limits the bandwidth. Practically, the compensation network can just consist of a capacitor in the range of 680 nF or 1 μF that is applied between pin3 and ground. Such a circuitry generates the following control characteristic:

$$\frac{V_{REGUL}}{V_{OUT}} = \frac{R_{fb2} \cdot G_{EA}}{s \cdot 3 \cdot (R_{fb1} + R_{fb2}) \cdot C_2} \quad \text{(eq. 32)}$$

Where:

- G_{EA} is the trans−conductance gain of the error amplifier (200 μS, typically)
- C_2 is the compensation capacitor (see Figure 5)
- R_{fb1} and R_{fb2} are the feedback resistors (see Figure 5)

Hence, we have them the following pole:

$$f_{p1} = \frac{1}{6\pi \cdot \frac{(R_{fb1}+R_{fb2})}{R_{fb2} \cdot G_{EA}} \cdot C_2} \quad \text{(eq. 33)}$$

In our case, we choose (C_2 = 680 nF) which leads to a

$$\left(\frac{1}{6\pi \cdot \frac{(4160\,k + 27\,k)}{27\,k \cdot 200\,\mu} \cdot 680\,n} \cong 0.1\ Hz \right)$$

corner frequency.

1. The circuit does not enable the under−shoots limitation function during the start−up sequence of the PFC stage but only once the converter has stabilized (that is when the “pfcOK” signal of the block diagram, is high). This is because, at the beginning of operation, the pin3 capacitor must charge slowly and gradually for a soft start−up.

Current Sense Network

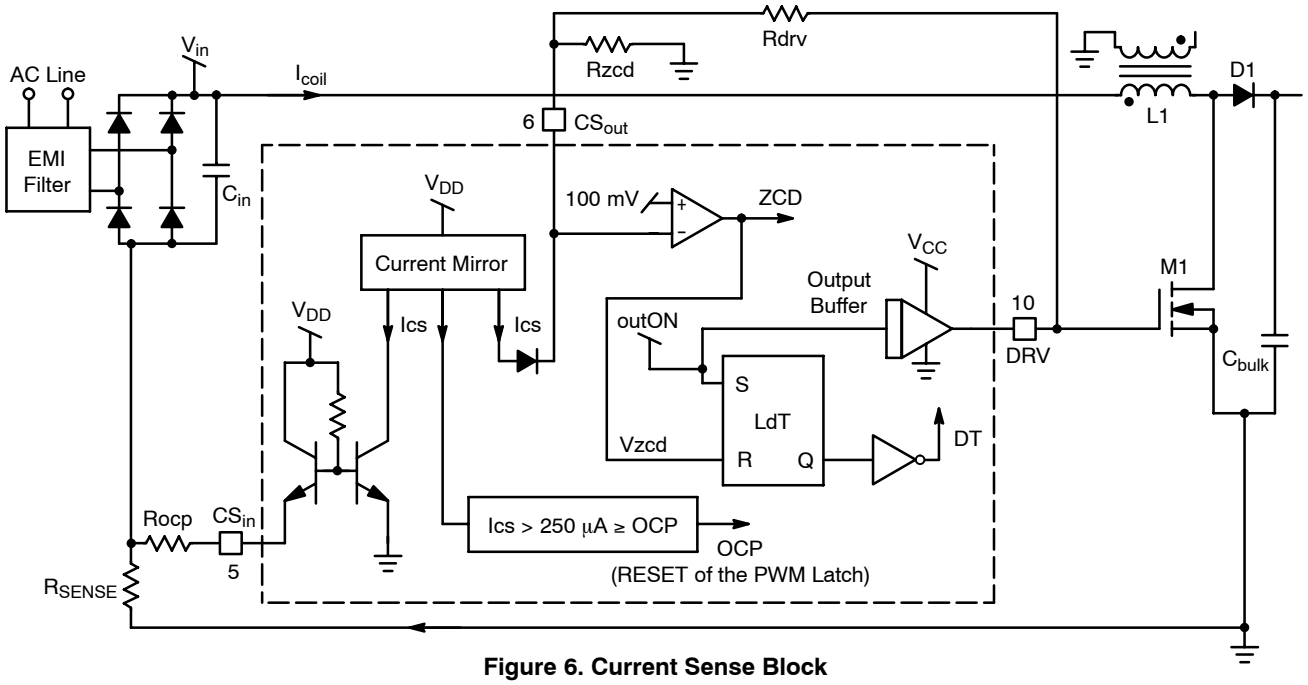

Figure 6. Current Sense Block

The CS block performs the over−current protection and the zero current detection.

The NCP1605 is designed to monitor a negative voltage proportional to the coil current. Practically, a current sense resistor (R_{SENSE} of Figure 6) is inserted in the return path to generate a negative voltage proportional to the coil current. The circuit incorporates an operational amplifier that sources the current necessary to maintain the CS pin voltage null (refer to Figure 6). By inserting a resistor R_{OCP} between the CS pin and R_{SENSE}, we adjust the pin5 current as follows:

$$-[R_{CS}I_{COIL}] + [R_{OCP}I_{pin5}] = V_{pin5} \approx 0 \quad \text{(eq. 34)}$$

Finally the pin5 current is proportional to the coil current as shown by the following equation:

$$I_{pin5} = \frac{R_{CS}}{R_{OCP}} I_{COIL} \quad \text{(eq. 35)}$$

In other words, the pin5 current is proportional to the coil current. The circuit uses I_{pin5} to set the coil current limit (Over−Current Protection). Practically, if Ipin5 exceeds 250 μA, the PWM latch is reset for a cycle by cycle current limitation. Hence, the maximum coil current is:

$$I_{COIL,MAX} = \frac{R_{OCP}}{R_{SENSE}} 250\ \mu A \quad \text{(eq. 36)}$$

Finally, the ratio (R_{OCP} / R_{SENSE}) sets the over−current limit in accordance with the following equation:

$$\frac{R_{OCP}}{R_{SENSE}} = \frac{I_{COIL,MAX}}{250\ \mu A} \quad \text{(eq. 37)}$$

As we have two external components to set the current limit (R_{OCP} and R_{SENSE}), the current sense resistor can be optimized to have the ***best trade−off between losses and noise immunity***.

As shown in [1], the R_{SENSE} losses are given by the following equation:

$$P_{RSENSE} = \frac{4 \cdot R_{SENSE}}{3} \cdot \left(\frac{P_{in,av}}{V_{in,rms}} \right)^2 \quad \text{(eq. 38)}$$

One can choose R_{SENSE} as a function of its relative impact on the PFC stage efficiency at low line and full power.

If α is the relative percentage of the power that can be consumed by R_{SENSE}, this criterion leads to:

$$\alpha \cdot (P_{in,av})_{max} = \frac{4 \cdot R_{SENSE}}{3} \cdot \left(\frac{(P_{in,av})_{max}}{(V_{in,rms})_{min}} \right)^2 \quad \text{(eq. 39)}$$

Finally:

$$R_{SENSE} = \frac{3 \cdot \alpha}{4} \cdot \frac{(V_{in,rms})_{min}^{\ 2}}{(P_{in,av})_{max}} \quad \text{(eq. 40)}$$

And:

$$R_{OCP} = R_{SENSE} \cdot \frac{I_{COIL,MAX}}{250\ \mu A} \quad \text{(eq. 41)}$$

In our application, we choose (α = 0.25%),

$$R_{SENSE} = \frac{3 \cdot 0.25\%}{4} \cdot \frac{90^2}{175} \cong 87\ m\Omega \quad \text{(eq. 42)}$$

In practice, we will use (R_{SENSE} = 0.1 Ω) and hence, since the maximum coil current is 6 A (see inductor computation):

$$R_{OCP} = 0.1 \cdot \frac{6\ A}{250\ \mu A} = 2.4\ k\Omega \quad \text{(eq. 43)}$$

Please note that R_{OCP} should not exceed 5 kΩ.

If your calculation led to an excessive R_{OCP} value, reduce R_{SENSE} to meet the aforementioned requirement.

The pin5 current is internally copied and sourced by pin6. Place a resistor (R_{pin6}) between pin6 and ground to build a voltage proportional to the coil current. The circuit detects the core reset when V_{pin6} drops below 100 mV, typically.

It is recommended to implement a zero current detection resistor on pin 6 (R_{ZCD}) that is as high as possible but that does not exceed 3 times R_{OCP}.

In addition, a resistor is to be placed between the drive output (pin9) and pin6, to ease the circuit detection by creating some over−riding at the turn on instant. It should be 3 times the R_{ZCD} to cope with all possible V_{CC} levels (V_{CC} and hence, the drive amplitude can range from 8 to 20 V).

$$R_{ZCD} = 3 \cdot R_{OCP} \quad \text{(eq. 44)}$$

$$R_{DRV} = 3 \cdot R_{ZCD} \quad \text{(eq. 45)}$$

Finally, in our application, we use:

$$R_{SENSE} = 100\ m\Omega \quad \text{(eq. 46)}$$

$$R_{OCP} = 2.4\ k\Omega \quad \text{(eq. 47)}$$

$$R_{ZCD} = 7.2\ k\Omega \quad \text{(eq. 48)}$$

$$R_{DRV} = 22\ k\Omega \quad \text{(eq. 49)}$$

The propagation delay (Vpin6 lower than 100 mV) to (drive output high) has been minimized (120 ns typically) to help turn on at the valley of the MOSFET drain−source voltage.

Over−Voltage Protection

The NCP1605 dedicates one specific pin for the under−voltage and over−voltage protections. The NCP1605 configuration allows the implementation of two separate feed−back networks (see Figure 8):

- One for regulation applied to pin 4 (feed−back input).
- Another one for the OVP function.

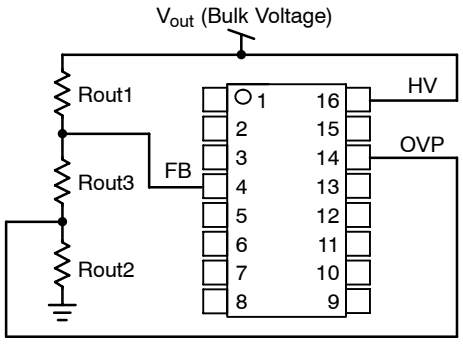

Figure 7. Configuration with One Feed−back Network for Both OVP and Regulation

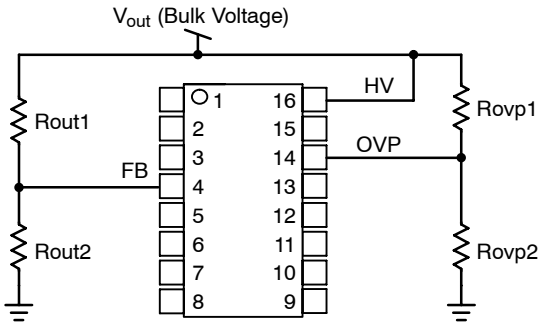

Figure 8. Configuration with Two Separate Feed−back Networks

The double feed−back configuration offers some redundancy and hence, an up−graded safety level as it protects the PFC stage even if there is a failure of one of the two feed−back arrangements.

However, the regulation and the OVP function have the same reference voltage (V_{REF} = 2.5 V) so that if wished, one single feed−back arrangement is possible as portrayed by Figure 7. The regulation and OVP blocks having the same reference voltage, the resistance ratio Rout2 over Rout3 adjusts the OVP threshold. More specifically,

– The bulk regulation voltage is:

$$V_{OUT} = \frac{Rout1 + Rout2 + Rout3}{Rout2 + Rout3} \cdot V_{REF} \quad \text{(eq. 50)}$$

– The OVP level is:

$$V_{OVP} = \frac{Rout1 + Rout2 + Rout3}{Rout2} \cdot V_{REF} \quad \text{(eq. 51)}$$

– The ratio OVP level over regulation level is:

$$\frac{V_{OVP}}{V_{OUT}} = 1 + \frac{Rout3}{Rout2} \quad \text{(eq. 52)}$$

For instance, (V_{OVP} = 105% · V_{OUT}) leads to the following constraint: (Rout3 = 5% · Rout2).

As soon and as long as the circuit detects that the output voltage exceeds the OVP level, the power switch is turned off to stop the power delivery.

In our application, the option that consists of two separate V_{OUT} sensing networks is chosen (as sketched by Figure 8). Like for the regulation network, the impedance of the monitoring resistors must be:

1. high enough to limit the losses that if excessive, may not allow to comply with the stand−by requirements to be met by most power supplies
2. low enough for a good noise immunity

Again, a bias current in the range of 100 μA generally gives a good trade−off.

Hence:

$$Rovp2 = \frac{V_{REF}}{100\ \mu A} = 25\ k\Omega \quad \text{(eq. 53)}$$

In practice, we can choose: R_{ovp2} = 27 kΩ (instead of 25 kΩ, 27 kΩ being a normalized value)

Finally,

$$Rovp2 = 27\ k\Omega \quad \text{(eq. 54)}$$

$$Rovp1 = Rovp2 \cdot \left(\frac{V_{OVP}}{V_{REF}} - 1\right) \quad \text{(eq. 55)}$$

In our application, we target an OVP level in the range of 410 V.

Hence,

$$Rovp2 = 27\ k\Omega \quad \text{(eq. 56)}$$

$$Rovp1 = 27\ k\Omega \cdot \left(\frac{410}{2.5} - 1\right) = 4401\ k\Omega \quad \text{(eq. 57)}$$

For safety reason, several resistors should be placed in series instead of a single Rovp1 one. In our application, we choose a (1800 kΩ + 1800 kΩ + 820 kΩ) network.

This selection together with (Rovp2 = 27 kΩ) leads to:

$$V_{OVP} = \frac{Rovp1 + Rovp2}{Rovp2} \cdot V_{REF} = \frac{1800\ k + 1800\ k + 820\ k + 27\ k}{27\ k} \cdot 2.5\ V \cong 412\ V \quad \text{(eq. 58)}$$

Maximum Power Adjustment

From the data−sheet equations, we can deduct the following expression of the instantaneous line current that is absorbed by the PFC stage:

$$I_{IN}(t) = \frac{C_{pin7} \cdot V_{REGUL} \cdot V_{OUT,nom}^{\ 2}}{2 \cdot 375\ \mu \cdot L \cdot V_{OUT}^{\ 2}} \cdot V_{IN}(t) \quad \text{(eq. 59)}$$

Where:

– (V_{REGUL}) is an internal signal linearly dependant of the output of the regulation block ($V_{CONTROL}$). (V_{REGUL}) varies between 0 and 1 V.
– $I_{IN}(t)$ and $V_{IN}(t)$ are the instantaneous line current and voltage respectively.
– L is the coil inductance
– $V_{OUT,nom}$ is the output regulation voltage. This level is set to about 390 V typically.

Equation (59) illustrates that as any voltage mode controller, the timing capacitor (C_{PIN7}) adjusts the power.

Multiplying I_{IN} by V_{IN} and averaging the result over the line period, the mean input power is deducted as follows:

$$P_{IN,AVG} = \frac{C_{pin7} \cdot V_{REGUL} \cdot V_{OUT,nom}^{\ 2}}{750\ \mu \cdot L \cdot V_{OUT}^{\ 2}} \cdot V_{IN,rms}^{\ 2} \quad \text{(eq. 60)}$$

Finally, since the maximum power is obtained when V_{REGUL} is 1 V:

$$(P_{IN,AVG})_{max} = \frac{C_{pin7} \cdot V_{OUT,nom}^{\ 2}}{750\ \mu \cdot L \cdot V_{OUT}^{\ 2}} \cdot V_{IN,rms}^{\ 2} \quad \text{(eq. 61)}$$

Now, as

$$V_{OUT,nom} = \frac{R_{fb1} + R_{fb2}}{R_{fb2}} \cdot V_{REF}$$

where V_{REF} is the regulation reference voltage (2.5 V) and R_{fb1} and R_{fb2} are the feed−back resistors as portrayed in Figure 5.

Hence, the input power can be expressed as follows:

$$P_{IN,AVG} = \left(\frac{R_{fb1} + R_{fb2}}{R_{fb2}}\right)^2 \cdot \frac{C_{pin7} \cdot V_{REGUL}}{120\ \mu \cdot L} \cdot \frac{V_{IN,rms}^{\ 2}}{V_{OUT}^{\ 2}} \quad \text{(eq. 62)}$$

The maximum power is only dependent on the coil inductance, on the input voltage magnitude and on the Cpin7 capacitor. $P_{IN,AVG}$ is also a function of the output voltage square so that the power capability of the PFC stage increases while V_{out} decreases. This is what allows the

Follower Boost characteristic (see data sheet for more information on this mode). If this operation mode is not wished (as this is the case in our application), the timing capacitor (C_{PIN7}) must be dimensioned so that the PFC stage can provide the full power at low line ($V_{IN,RMS} = [V_{IN,RMS}]_{LL}$) under the nominal output voltage ($V_{OUT} = V_{OUT,nom}$). The maximum V_{REGUL} value being 1 V, this leads to:

$$C_{pin7} = \frac{120\,\mu \cdot L \cdot (P_{IN,AVG})_{max}}{\left(\frac{R_{fb1}+R_{fb2}}{R_{fb2}}\right)^2} \cdot \frac{V_{OUT,nom}{}^2}{(V_{IN,RMS})_{LL}{}^2} \quad \text{(eq. 63)}$$

Noting that ,

$$V_{OUT,nom} = \frac{R_{fb1} + R_{fb2}}{R_{fb2}} \cdot V_{REF}$$

the above equation simplifies as follows:

$$C_{pin7} = \frac{120\,\mu \cdot L \cdot V_{REF}{}^2 \cdot (P_{IN,AVG})_{max}}{(V_{IN,RMS})_{LL}{}^2} \quad \text{(eq. 64)}$$

In our case,

- L = 150 μH
- $(P_{IN,AVG})_{max}$ = 190 W
- $(V_{IN,RMS})_{LL}$ = 90 V
- V_{REF} = 2.5 V

Hence:

$$C_{pin7} = \frac{120\,\mu \cdot 150\,\mu \cdot 2.5^2 \cdot 190}{(90)^2} \cong 2.64\ \text{nF} \quad \text{(eq. 65)}$$

Offsetting the pin7 Pin…

At high line, the PFC MOSFET on−time becomes very small and the circuit must be able to operate with low $V_{CONTROL}$ levels. At light load, these levels are particularly and make the circuit task very tough (the PWM comparator functions with very low inputs). To avoid excessive minimum on−times able to prevent the PFC stage to regulate when at high line and light load, skip mode is not activated, it is recommended to generate an offset on pin7 by placing a resistor R2 between Cpin7 and ground and forcing some voltage across R2 using the drive pulses (thanks to the resistor R8 of the application schematic).

The offset should be as high as 400 or 500 mV.

In our case, V_{CC} and hence, the drive pulses' amplitude is 15 V.

The choice of (R2 =150 Ω) together with (R8 = 4700 Ω) leads to a 460 mV offset. The maximum pin7 swing that is 1 V without offset, is now: 540 mV that is 54% of its normal value.

To allow the same maximum on−time, Cpin7 must be increased in response to this swing diminution as follows:

$$C_{pin7} = \frac{2.64\ \text{nF}}{54\%} = 4.9\ \text{nF} \quad \text{(eq. 66)}$$

Finally, the following timing network is implemented:

- Cpin7 = 4.7 nF
- R2 = 150 Ω
- R8 = 4.7 kΩ

Feeding Circuitry

The NCP1605 must start first and allow the downstream converter to operate when the output voltage of the PFC stage is nominal. This is done as follows:

- The NCP1605 start−up current source charges the V_{CC} capacitor tank that is common to the two controllers (NCP1605 and NCP1217A). As the NCP1605 V_{CC} start−up level is high (15 V typically while the NCP1217A starts to operate when its supply voltage exceeds 12.8 V typically), V_{CC} is necessarily high enough to activate both drivers when the start−up current source turns off.
- The circuitry of Figure 9 is implemented to power the two controllers after start−up. An auxiliary winding is added across the forward transformer (see Figure 9). The turn ratio is 1/14. The diode D_{15} rectifies the ac voltage seen by the auxiliary winding so that the capacitor C_{28} is substantially charged to (V_{BULK}/14), i.e., about 28 V when the MOSFETs X31 and X24 are on. A low cost regulator consisting of Q7, R31, D9 and D8 steps down this voltage to provide both the NCP1605 and NCP1217A with a friendly voltage (around 15 V).

This configuration that makes C28 store a significant amount of energy as soon as there is some activity in the forward side (C28 being charged up to almost 30 V), allows a robust powering of the controllers even in stand−by where they enter skip−cycle mode to reduce the losses.

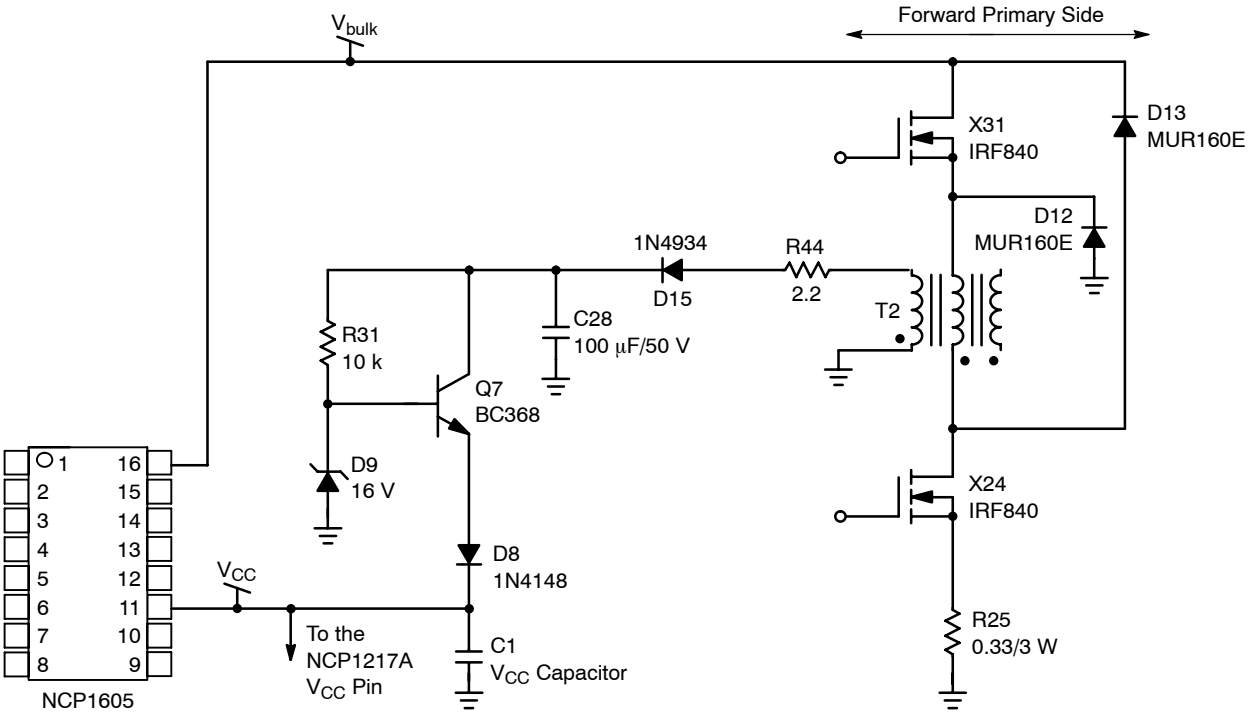

Figure 9. Feeding Circuitry

Stand−by Management

The NCP1605 automatically skips switching cycles when the power demand drops below a given level. This is accomplished by monitoring the pin1 voltage that must receive a voltage below 300 mV in light load conditions. Practically, a portion of the feedback signal of the downstream converter is applied to pin 1, as portrayed by Figure 10.

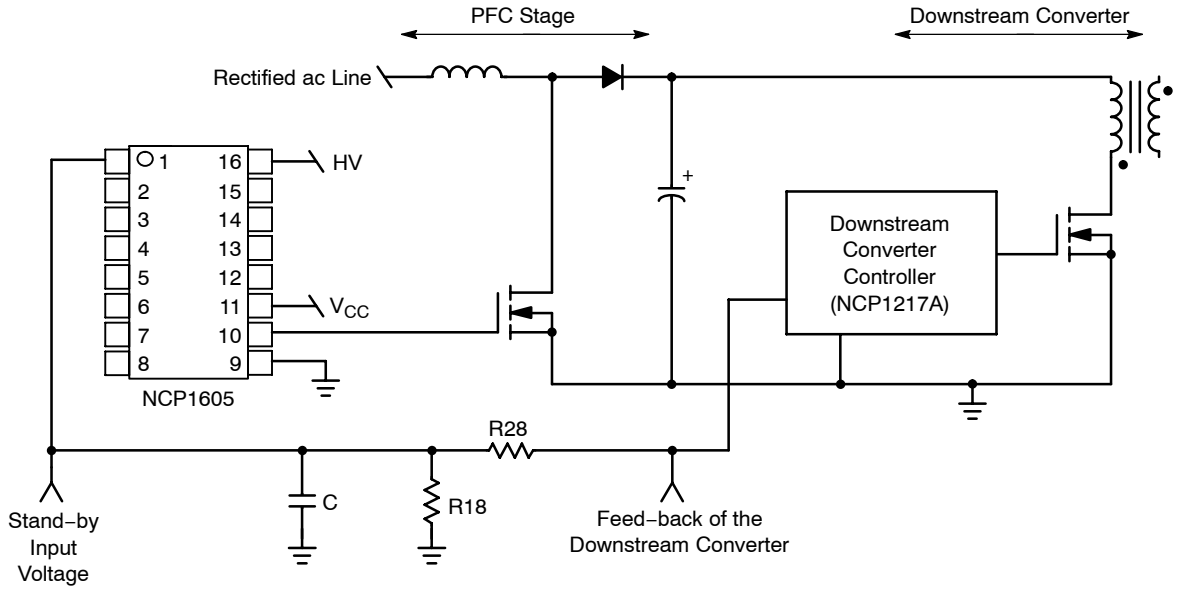

Figure 10. Signal for Stand−by Detection

A portion of the SMPS feedback is injected to pin1. In our application, R28 is 47 kΩ and R18 is 22 kΩ so that 30% of the SMPS feedback voltage is applied.

In normal operation, the circuit controls the ***continuous*** absorption of the line current necessary for matching the load power demand. Instead, when the voltage applied to pin1 goes below 300 mV:

- The output pulses are blanked and pin3 ("$V_{CONTROL}$") is grounded,
- The output of the PFC stage being not fed any more, it drops. When the output voltage goes below 95.5% of

the regulation level, the circuit resumes operation until “FLAG1” becomes low (what means that the output voltage has exceeded the regulation level).

– At that moment, if Vpin1 is still below 300 mV, a new skipping phase starts.

In other words, instead of continuously providing the output with a small amount of power, the circuit operates from time to time at a higher power level. As an example and to make it simple, instead of continuously supplying 1% of P_{MAX}, the circuit can provide the load with 10% of P_{MAX} for 10% of the time. The IC enters the so−called skip cycle mode that is much more efficient compared to a continuous power flow as it drastically reduces the number of pulsations and therefore the switching losses associated to them. Figure 11 portrays this operation mode.

Remarks:

- This technique that is based on the monitoring of the downstream converter feed−back, makes the PFC stage enter the skip mode at a very stable power level over the input voltage range.
- When in skip mode, each working phase of the PFC stage, starts smoothly as pin3 is grounded at the beginning of it. This soft−start capability is effective to avoid the audible noise that could possibly result from such a burst operation.

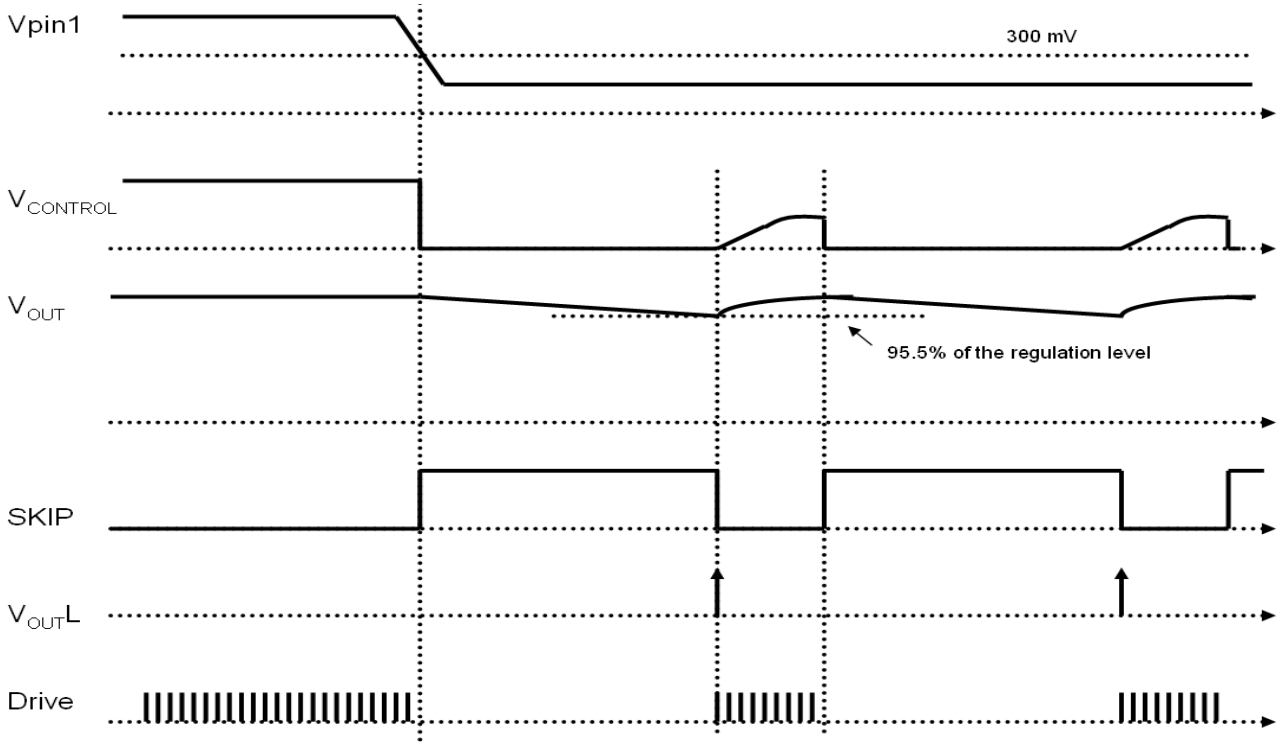

Figure 11. Stand−by Management

Control of the Downstream Converter (“pfcOK” Pin)

The signal “pfcOK/REF5V is high (5 V) when the PFC stage is in normal operation (its output voltage is stabilized at the nominal level) and low otherwise.

More specifically, “pfcOK/REF5V” is low:

- During the PFC stage start−up, that is, as long as the output voltage has not yet stabilized at the right level.
- In case of a condition preventing the circuit from operating properly, i.e., during the V_{CC} charge by the high voltage start−up current source, in brown−out conditions or when one of the following major faults sets the “Fault Latch” of the block diagram, causing the circuit turning off:
  - Incorrect feeding of the circuit (“UVLO” high when $V_{CC} < V_{CC}OFF$, $V_{CC}OFF$ equating 9 V typically).
  - Excessive die temperature detected by the thermal shutdown.
  - Under−Voltage Protection.
  - Too repetitive Over−Voltage conditions leading to the circuit shutdown (“STDWN” of the block diagram turns high).
  - A major fault has definitively latched off the circuit.

And “pfcOK/REF5V” is high when the PFC output voltage is properly and safely regulated. The signal is intended to control the operation of the downstream converter.

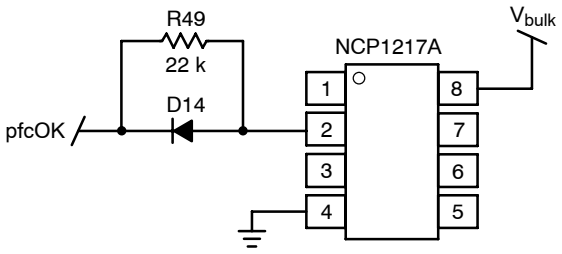

Figure 12. Enabling / Disabling the Downstream Converter

The signal “pfcOK” is low when the PFC stage is not in nominal operation (start−up, fault conditions) and high (5 V) when it is ok for operation.

The PFC controls the downstream converter activity thanks to the « pfcOK » signal:

- If ”pfcOK” is low, the NCP1217A feed−back is forced low by D14 and the forward does not operate
- If ”pfcOK” is high, the NCP1217A feed−back is no more grounded and the forward is free to operate.

R49 is optional. It is implemented here as an additional pull−up resistor that increases the biasing current on the NCP1217A feed−back pin. D14 could be removed if a resistor R49 was implemented that is low impedance enough to disable the controller when “pfcOK” is in low state.

Design of the Two−switch Forward

The NCP1605 enables the two−switch forward when the PFC stage output is nominal. Therefore, its input voltage range is narrow. More specifically, we will consider that:

- the minimum input voltage is 350 V (taking into account the 10 ms hold−up time)
- the maximum one is 450 V

We select the NCP1217A as the two−switch forward because it guarantees that the duty cycle cannot exceed 50%. Also, this compact and cost−effective circuit incorporates some stand−by management to keep the stand−by losses at a low level.

Selection of the Magnetic Components and of the Output Capacitor:

Two components are to be computed:

- the forward transformer that transfers the energy from the primary to the secondary side
- the output filtering coil that:
  - Adjusts the ripple of the output current. As a rule of the thumb, 70% of the maximum load current will be used as the peak to peak ripple.
  - In conjunction with the output capacitor filters the ac voltage provided by the transformer, to form the dc output voltage (19 V). (L.C) must be large enough to meet the ripple requirements of the 19 V output voltage.

Forward Transformer Design

Since the NCP1217A limits the duty−cycle at a level that can be as low as 42% (see data−sheet), the turn ratio of the forward transformer must selected so that the voltage it applies to the secondary side is high enough to provide 20 V (that is 19 V the output voltage + the diode voltage drop) when the bulk voltage is minimum (350 V). In other words:

$$\frac{N_S}{N_P} \cdot V_{BULK,min} > \frac{20\ V}{42\%}$$

Hence:

$$\frac{N_P}{N_S} < 42\% \cdot \frac{350}{20} = 7.35$$

A 7 ratio is selected, that gives some margin.

The magnetizing inductor is selected in order to minimize the ($L \cdot I_{pk}^2$). The choice of the output current ripple leads to a 800 μH inductor.

Finally, a ETD39, ferrite core transformer is implemented. A third winding (auxiliary winding) is added for the V_{CC} generation (see the “feeding circuitry” section). We choose ($N_P / N_{AUX} = 14$) so that the auxiliary winding provides about 28 V when the bulk voltage nominal.

Finally, the transformer specification is:

- L_P = 800 μH
- $N_P / N_S = 7$
- $N_P / N_{AUX} = 14$
- $I_{P,RMS}$ = 1,9 A
- $I_{P,MAX}$ = 3 A
- $I_{S,RMS}$ = 9.5 A
- $I_{S,MAX}$ = 11 A

Design of the Output Filtering Network

The criterion 1 (70% current ripple) leads to:

$$\Delta I_{COIL} = 70\% \cdot I_{LOAD,MAX} = 70\% \cdot 8\ A = 5.6\ A$$

On the other hand:

$$\Delta I_{COIL} = \frac{V_{BULK}/7}{L} \cdot \frac{V_{out} + V_F}{V_{BULK}/7 + V_F} \cdot 7.5\ \mu s \rightarrow$$

$$L \cong \frac{19 + 1}{5.6} \cdot 7.5\ \mu s = 26\ \mu H$$

Two parallel low ESR, 470 μF / 25 V capacitors are connected across the output to form the output (L, C) filter together with the 26 μH / 11 A inductor.

Application Schematics

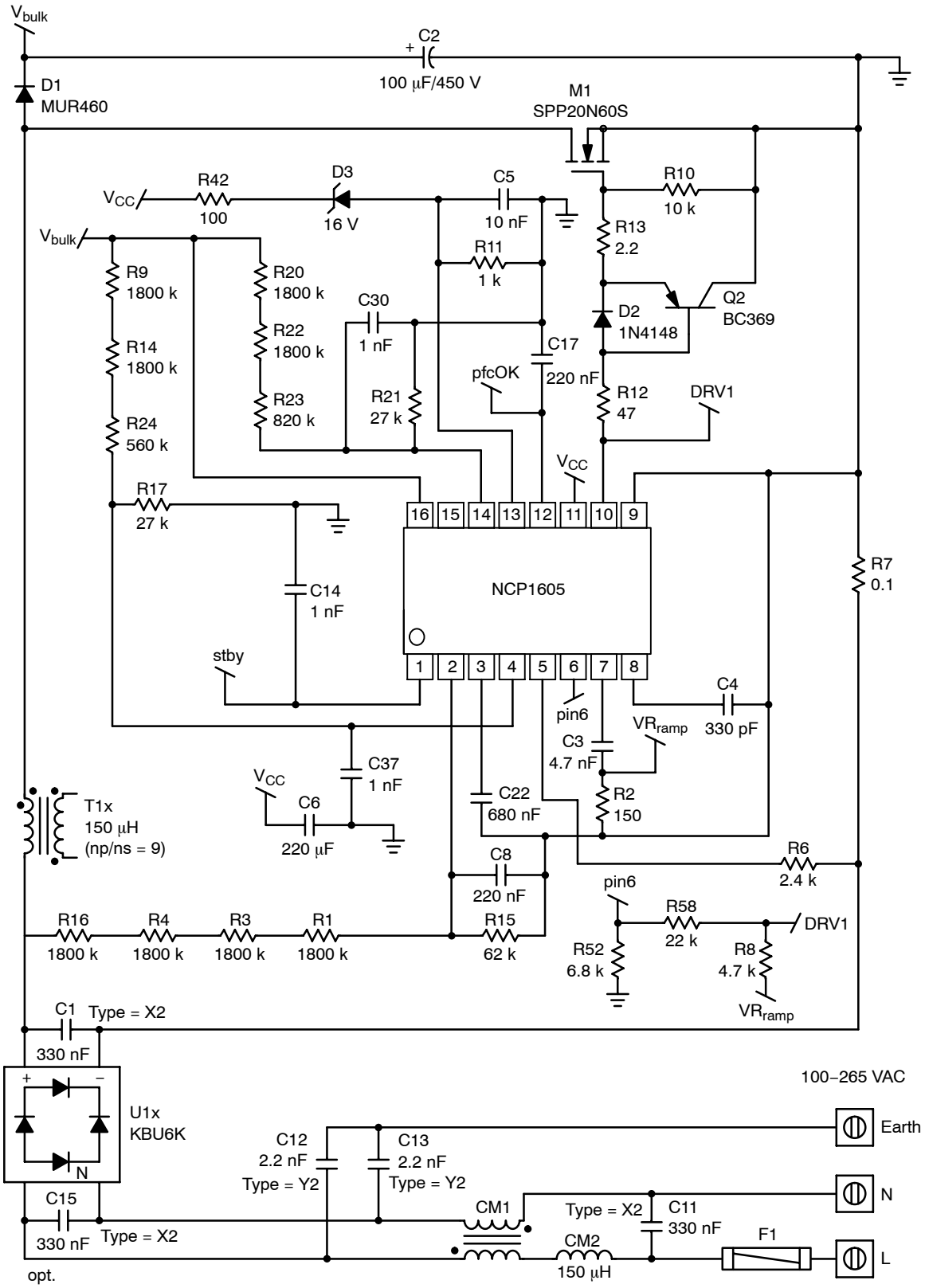

Figure 13. PFC Stage

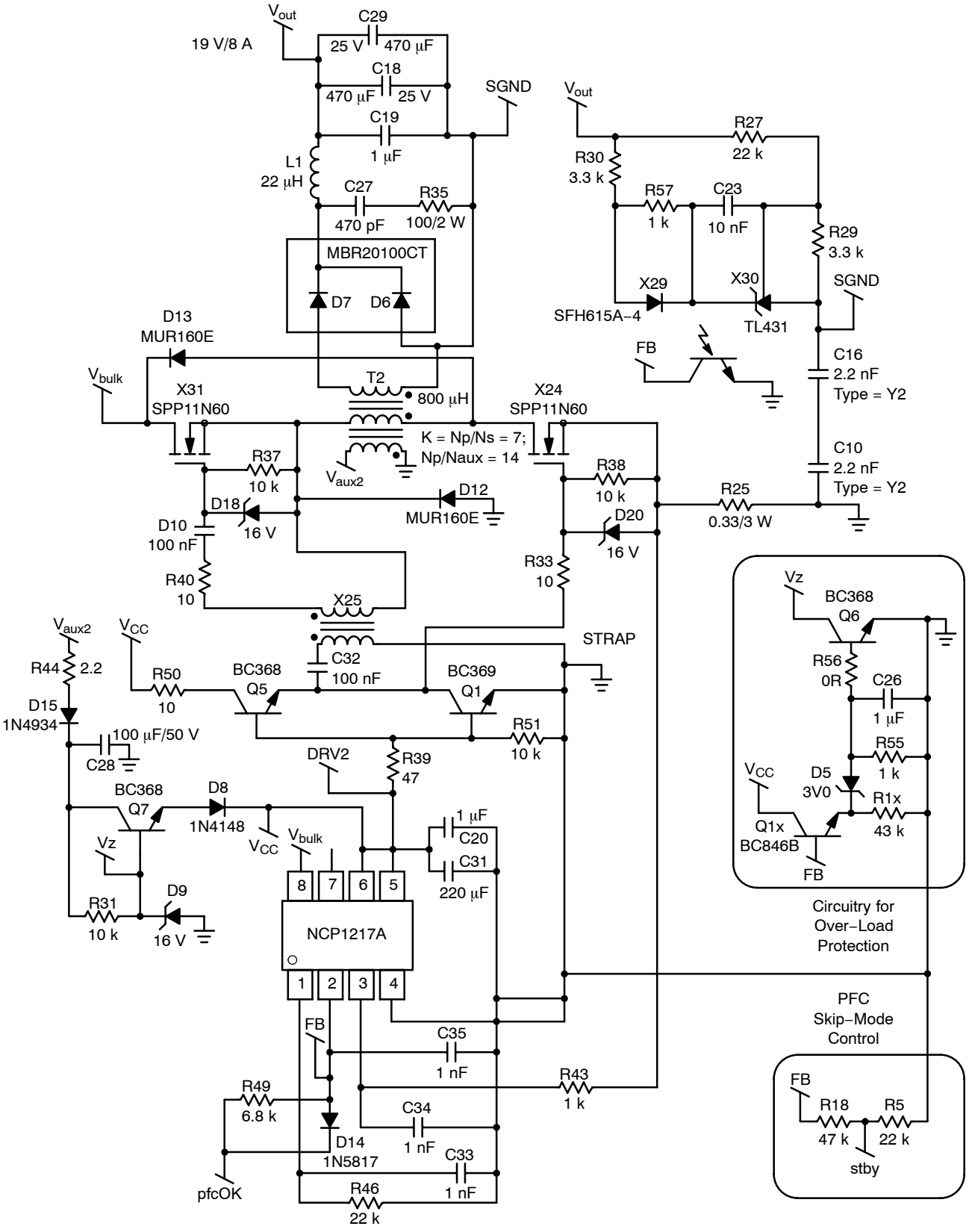

Figure 14. Forward Stage

Bill of Materials

CM1	CM CHOKE	B82734−R2322−B30	EPCOS
CM2	DM CHOKE	WI−FI series − 150 μH	Wurth Electronik
C1, C11, C15	330 nF X2 Capacitor	PHE840MY6330M	RIFA
C2	Bulk Cap. 100 μF / 450 V	222, 215, 937, 101	BC Components
C3	CMS Capacitor	4.7 nF	various
C4	CMS Capacitor	330 pF	various
C5, C8, C17	CMS Capacitor	220 nF	various
C6, C31	Electrolytic Capacitor	220 μF / 25 V	various
C14, C33, C34, C35, C30, C37	CMS Capacitor	1 nF	various
C27	CMS Capacitor	470 pF	various
C21, C25, C12, C13	2.2 nF Y2 Capacitor	DE2E3KH222MA3B	muRata
C18, C29	electrolytic Capacitor	UPM1E471MPD	Nichicon
C19, C20	CMS Capacitor	1 μF	various
C22, C26	CMS Capacitor	680 nF	various
C23	CMS Capacitor	10 nF	various
C28	Electrolytic Capacitor	100 μF / 50 V	various
C32	CMS Capacitor	100nF	various
D10	Through Hole Ceramic Cap	100 nF	various
C38	CMS Capacitor	330 nF	various
D1	PFC Diode	MUR460RLG	ON Semiconductor
D2, D8	DO−35 Diode	1N4148	various
D14	Schottky Diode	1N5817	ON Semiconductor
D3, D9	16 V Zener Diode	1N5930	ON Semiconductor
D18, D20	16 V Zener Diode	BZX84C16LT1, G	ON Semiconductor
D16	16 V Zener Diode	BZX79−C3V0	ON Semiconductor
D6, D7	Dual Schottky Diode	MBR20100CT	ON Semiconductor
D12, D13	Demagnetization Diodes	MUR160RLG	ON Semiconductor
D15	Rectifier	1N4934RLG	ON Semiconductor
HS1_M1, HS3_D6	Heatsink	KL195/25.4SW	Schaffner
HS1_X31, HS2_X24	Heatsink	KL194/25.4SW	Schaffner
L1	DMT2−26−11L	26 μH Power Choke	CoilCraft
M1	PFC MOSFET	SPP20N60S5	Infineon
Q1, Q2	PNP TO92 Transistor	BC369	ON Semiconductor
Q1x	SOT23	BC846B	ON Semiconductor
Q5, Q6, Q7	NPN TO92 transistor	BC368	ON Semiconductor
R1, R3, R4, R9, R14, R16, R20, R22	1%, 1/4 W Resistors	1.8 MR	various
R2	1%, 1/4 W Resistors	150 R	various
R12, R39	1%, 1/4 W Resistors	47 R	various
R6	1%, 1/4 W Resistors	2.4 kR	various
R7	3 W PFC CS Resistor	RLP3 0R1 1%	Vishay
R8	1%, 1/4 W Resistors	4.7 k	various
R10, R31, R37, R38, R51	1%, 1/4 W Resistors	10 kR	various
R13, R44	1%, 1/4 W Resistors	2.2 R	various
R15	1%, 1/4 W Resistors	62 kR	various
R17, R21	1%, 1/4 W Resistors	27 kR	various
R18, R27, R46, R58	1%, 1/4 W Resistors	22 kR	various
R23	1%, 1/4 W Resistors	820 kR	various
R24	1%, 1/4 W Resistors	560 kR	various
R25	3 W 0.39 R Forward CS Resistor	W31−R39 JI	WELWYN
R33, R40, R50	1%, 1/4 W Resistors	10 R	various

Bill of Materials

R28, R55	1%, 1/4 W Resistors	47 kR	various
R29, R30	1%, 1/4 W Resistors	3.3 kR	various
R35	100 R / 4 W Resistor	SBCHE4	Meggitt CGS
R11, R43, R57	1%, 1/4 W Resistors	1 kR	various
R42	1%, 1/4 W Resistors	100 R	various
R49, R52	1%, 1/4 W Resistors	6.8 k	various
R1x	1%, 1/4 W Resistors	43 k	various
T1	PFC Coil	SICO 977	Sicoenergie
T2	Forward Transformer	SICO 978	Sicoenergie
U1	Diodes Bridge	KBU6K	General Semiconductor
U2	Forward Controller	NCP1217AD133R2G	ON Semiconductor
U3	PFC Controller	NCP1605	ON Semiconductor
X25	01:01 Pulse Transformer	Q3903−A	CoilCraft
X29	Opto−coupler	SFH6156−2	Infineon
X30	TO92 Voltage Reference	TL431ACDR2G	ON Semiconductor
X24, X31	Forward MOSFET	SPP11N60S5	Infineon
F1	4 A Fuse	various	various

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